01-31-05

Thru AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Summerer	Docket No.:	99 P 7719 US 02
Serial No.:	09/733,665	Art Unit:	2128
Filed:	January 28, 2005	Examiner:	Thai Q. Phan
For:	Semiconductor Structures and Manufacturing Methods		

Certificate of Mailing via Express Mail

EXPRESS MAIL mailing label number: EV 552629342 US

Date of Deposit: January 28, 2005

I hereby certify that the following documents, which are enclosed, are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450:

Certificate of Mailing via Express Mail (1 page)
Fee Transmittal (1 original and 1 copy = 2 pages)
Appeal Brief (in triplicate (13 pages each = 39 pages)
Two (2) Return Postcards

Respectfully submitted,

Julie Russell
Legal Assistant

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252-5793
Tel: 972-732-1001
Fax: 972-732-9218

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/733,665
Filing Date	December 8, 2000
First Named Inventor	Summerer
Examiner Name	Thai Q. Phan
Art Unit	2128
Attorney Docket No.	99 P 07719 US 02

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 50-1065

Deposit Account Name: Slater & Matsil, L.L.P.

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	-20**=		X		=	
Independent Claims	- 3**=		X		=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

** or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	495	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	500.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,370	2453	685	Petition to revive – unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
				Other fee (specify)	

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 500.00

SUBMITTED BY

Complete *(if applicable)*

Name (Print/Type)	Ira S. Matsil	Registration No. (Attorney/Agent)	35,272	Telephone	972-732-1001
Signature				Date	January 28, 2005

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Summerer	Docket No.:	99 P 07719 US 02
Filed:	December 8, 2000	Examiner:	Thai Q. Phan
Serial No.:	09/733,665	Art Unit:	2128
For:	Semiconductor Structures and Manufacturing Methods		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed July 29, 2004. A Notice of Appeal was filed by facsimile on November 29, 2004.

REAL PARTY OF INTEREST

The present application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals or interferences.

STATUS OF THE CLAIMS

Claims 4-17 stand finally rejected. No claims have been allowed. Claims 1-3 were canceled in view of a restriction requirement in the patent application. The claims on appeal are reproduced in the attached Appendix.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to final rejection.

SUMMARY OF THE INVENTION

The present invention relates to an apparatus for detecting an alignment mark on a semiconductor body. Page 4, line 10.[1] The apparatus is particularly useful with an alignment mark 102 that includes two sets of parallel lines 112 and 114 configured in an overlying relationship that are disposed on the semiconductor body (e.g., wafer 104).[2] As shown in Figure 6, the parallel lines 112 in one of the sets are orthogonal to the parallel lines 114 in the other set.

As discussed in the Background of the Invention, a typical prior art alignment site on a semiconductor body includes two marks 13 and 15, as shown in Figure 2. Page 2, line 22. *See also* Nishi, Figure 2b. The mark 13 has lines oriented at +45 degrees while the mark 15 has lines oriented at -45 degrees. Page 2, line 23. Figure 1 shows a prior art alignment system that can be used in conjunction with a wafer that includes marks 13 and 15. Page 1, line 10. Using the system of Figure 1, the marks 13 and 15 are sequentially scanned by a cross-shaped light beam from alignment illumination 10. Page 2, line 11. A detector arrangement includes detectors 22_1 and 22_2 to detect light from the first mark 13 and detectors 22_3 and 22_4 to detect light reflected from the second mark 15. Page 2, lines 14-21. These detectors are activated and deactivated depending upon which orientation alignment mark is being illuminated. Page 3, line 10.

The alignment marks of the preferred embodiment also include two sets of parallel lines, the

---

[1] The page and line numbers refer to related portions of the application for the purpose of showing support in the originally filed paper. Appellant makes no assertion that the cited portion is the only or even the most relevant reference.

[2] The Final Rejection argues that the configuration of the alignment mark is not part of the claimed apparatus. For this brief, Appellant accepts this conclusion.

lines of one set being orthogonal to the lines of the other set. See, e.g., Figure 6. Unlike the prior art alignment marks of Figure 2,[3] the two sets of parallel lines overlie one another. As such, sets of lines will be illuminated simultaneously. The present invention provides an apparatus that can be used to detect alignment marks of this sort.

In particular, the detection apparatus includes an optical system 204 for scanning an alignment illumination comprising a pair of orthogonal lines 208 and 210 of impinging light over the surface of the alignment mark. Page 6, lines 10-13. One of such pair of impinging light lines 208 is orthogonal to and laterally displaced from the other one of such pair of impinging light lines 210. Page 6, lines 13-15. The impinging light 208/210 is reflected by the alignment lines in the surface of the semiconductor body 104 to provide a pair of laterally displaced beams of reflected light 211 and 213. Page 6, lines 18-21. The apparatus also includes a pair of laterally spaced detectors 220_1 and 220_2. Page 6, lines 22-23. Each one of the detectors 220_1 and 220_2 is positioned to detect a corresponding one of the laterally displaced beams of reflected light 213 and 211. Page 7, lines 11-14.

ISSUES

(1) Claim 4 requires an alignment illumination comprising a pair of orthogonal lines of impinging light and Nishi teaches an illumination comprising a single line of impinging light. Does the Nishi reference's disclosure of laterally spaced line patterns on a wafer teach or suggest laterally spaced lines of light?

(2) Claim 4 also requires a pair of laterally spaced detectors, each one of the detectors being positioned to detect a corresponding one of the laterally displaced beams of reflected light. Would

[3] See also Nishi, Figure 2b.

it be obvious to modify the apparatus taught by Nishi to include a pair of laterally spaced detectors when the Nishi system never teaches two laterally displaced beams of light?

(3) Claims 5-8, 14-15 and 17 depend from and further limit claim 4. Are these claims obvious in view of Nishi?

GROUPING OF THE CLAIMS

The groupings of claims that stand and fall together are listed below. The reasons for this grouping are clearly set forth in the arguments.

a. Claims 4, 9-13 and 16 stand or fall together.

b. Claims 5-7 stand or fall together.

c. Claim 8 stands or falls alone.

d. Claims 14-15 stand or fall together.

e. Claim 17 stands or falls alone.

ARGUMENTS

It is respectfully submitted that claims 4-17 recite patentable subject matter under the provisions of 35 U.S.C. § 103.

1. The Rejection

The Examiner finally rejected claims 4-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,411,386 to Nishi (hereinafter "Nishi" or "the Nishi reference"[4]).

[4] Throughout the Final Rejection, the cited prior art is referred to as "Kenji," which is the first name of inventor Kenji Nishi. To avoid confusion in this brief, each of the Final Rejections references to Kenji will be changed to Nishi.

To save space, these rejections will not be repeated here. Relevant aspects of the rejections will be discussed in the Appellant's arguments.

2. Appellant's Arguments

Appellant respectfully submits that each of the presently pending claims is allowable over the references of record. Each of the issues indicated above will now be addressed.

(1) Claim 4 requires an alignment illumination comprising a pair of orthogonal lines of impinging light and Nishi teaches an illumination comprising a single line of impinging light. Does the Nishi reference's disclosure of laterally spaced line patterns on a wafer teach or suggest laterally spaced lines of light?

Claim 4 specifically recites "an optical system for scanning an alignment illumination comprising a pair of orthogonal lines of impinging light over the surface of the alignment mark." This claim further recites that "one of such pair of impinging light lines [is] orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines." Appellant has studied the Nishi reference and can find no teaching of an illumination source that generates two laterally displaced light lines, much less the specific teachings of claim 4. Further, the Final Rejection points to no teaching on Nishi of a pair of impinging light lines.

To show that Nishi teaches the presently claimed invention, the Final Rejection states that the reference teaches an "alignment mark (24X and 24Y)[5] on the wafer surface comprising a pair of orthogonal lines in the X-Y direction and laterally displaced from the other for reflecting impinging light of the orthogonal lines of reticle R on the wafer marks." Final rejection, page 3. "In other words, this wafer mark with orthogonal and laterally spaced lines pattern is for reflecting impinging light beam of the orthogonal reticle R." *Id.*

---

[5] See e.g., Figure 2b.

While this statement may be true, Appellant is not sure how it is relevant. Claim 4 requires "a pair of orthogonal lines of impinging light." The Final Rejection cites to no portion of the reference that teaches or suggests a pair of orthogonal lines of impinging light. Marks on a wafer cannot teach or suggest lines of light from an illumination source.

Appellant made this argument during prosecution. In response, the Final Rejection stated:

> [Nishi] optical scanning system is for scanning (Fig. 1, col. 6, lines 28-50) illumination light reflected from alignment mark (col. 8). "Thus, this alignment mark with feature as shown above is to reflect impinging light of lateral spaced and orthogonal lines as claimed (col. 8, reticle pattern of X-Y orthogonal lines). Nishi also discloses pairs of orthogonal lines on wafer marks to reflect impinging light from illumination image light source (col. 7, lines 56-65), and laterally displaced from the other one of such pair (24X and 24Y) to provide a pair of orthogonal lines of reflected and laterally displaced impinging lights (Figs. 2, col. 8, lines 5-22, col. 10, lines 22-35, for example).

Final Rejection, page 6.

Once again, Appellant notes that the claim requires that the impinging light be provided in laterally displaced light lines. The Final Rejection's showing that the reference teaches laterally displaced alignment marks is not relevant. As taught in one of the sections cited by the Examiner, "[t]he alignment sensor 4 has an illuminating system for illuminating the mark to be examined with white light." Nishi, Col. 7, lines 56-58. There is no indication that this white light is provided as a pair of orthogonal lines of light or that this white light is provided as laterally displaced lines of light.

Since the reference does not teach a claimed limitation and the Final Rejection provides no rationale as to why this limitation would be an obvious modification, Appellant respectfully submits that claim 4 is allowable over the references of record.

(2) Claim 4 also requires a pair of laterally spaced detectors, each one of the detectors being positioned to detect a corresponding one of the laterally displaced beams of reflected light. Would it be obvious to modify the apparatus taught by Nishi to include a pair of laterally spaced detectors when the Nishi system never teaches two laterally displaced beams of light?

Claim 4 also requires "a pair of laterally spaced detectors, each one of the detectors being positioned to detect a corresponding one of the laterally displaced beams of reflected light." It is undisputed that Nishi does not teach a pair of laterally spaced detections. Final Rejection, page 4 (stating "[Nishi] does not expressly disclose a pair of detectors spaced laterally to detect reflected light as claimed"). The Final Rejection concludes, however, that such a modification of the reference would have been obvious based upon the following rationale.

> It would have been obvious for practitioner in the art at the time of the invention was made to find [Nishi] detector having CCD-type two dimensional (array) image sensor implied the claimed limitation of pair of detectors spaced laterally because typical CCD-type two dimensional image sensor has an array of sensing elements, or at least a pair of sensors as claimed, arranged in two dimension usually lateral spacing, for detecting signals reflected from the illuminated wafer mark.

Final Rejection, page 4.

Appellant respectfully submits that it would not have been obvious to modify the detector taught by Nishi to detect laterally displaced beams of reflected light since Nishi's apparatus never generates laterally displaced beams of light. Appellant acknowledges that one of ordinary skill in the art would know how to produce a detector for laterally displaced beams of light. However, one reading the teachings of Nishi would have no reason to build such a detector. What would motivate one to include a detector that detects two beams in a system that only generates one beam of light? It is clear that no such motivation exists. Therefore, claim 4 cannot be obvious in view of Nishi.

(3) Claims 5-8, 14-15 and 17 depend from and further limit claim 4. Are these claims obvious in view of Nishi?

a. Claims 5-7

Claim 5 specifically requires that "a first impinging light line is projected onto the wafer surface at an angle of -45° with respect to a Y axis" and claim 6, which depends from claim 5, requires that "a second impinging light line is projected onto the wafer surface at an angle of +45° angle with respect to the Y axis." Appellant respectfully submits that these claims are allowable over the Nishi reference.

As discussed above, Nishi never teaches or suggests a first impinging light line and a second impinging light line. Nishi certainly never teaches that the first impinging light line is projected on the wafer surface at an angle of -45° and the second impinging light line is projected onto the wafer surface at an angle of +45°.

The Final Rejection states that Nishi discloses an impinging light beam and that it would be obvious "to arrange the wafer mark and optical scanning beam in the claimed direction to detect wafer alignment." This conclusory statement finds no support in the teachings of the Nishi reference. Appellant respectfully submits that a rejection that merely restates the claim without citing to a reference, or providing additional support, cannot be maintained. Simply stated, claims 5 and 6 claim subject matter that is not taught or suggested by the prior art.

b. Claim 8

Claim 8 specifically requires that "the alignment marks are scanned first by the light line with +45° orientation and subsequently by the line with -45° orientation." To reject this claim, the Final Rejection merely states that "[Nishi] teaches alignment marks with features above would imply the claimed limitations to detect wafer mark alignment on the semiconductor body."

However, Nishi does not teach or suggest the limitations of claim 8. Since the reference does not teach the claimed limitations, and the Final Rejection has provided no rationale as to any modification to the prior art could be made, Appellant respectfully submits that claim 8 is allowable.

c. Claims 14-15

Claim 14 specifically requires that "a first detector configuration comprises a first detector for detecting left +45° and a second detector for detecting right +45° lines." To reject this claim, the Final Rejection merely states that "[Nishi] teaches alignment marks with features above would imply the claimed limitations to detect wafer mark alignment on the semiconductor body." However, Nishi does not teach or suggest the limitations of claim 14. The Final Rejection makes no attempt to argue otherwise. Since the reference does not teach the claimed limitations, and the Final Rejection has provided no rationale as to any modification to the prior art could be made, Appellant respectfully submits that claim 14 is allowable.

d. Claim 17

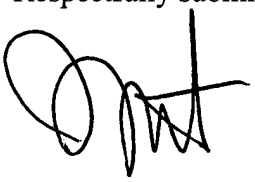
Claim 17 specifically requires that "the recorded waveforms are recorded without background noise from the other line orientation." To reject this claim, the Final Rejection merely states that "[Nishi] teaches alignment marks with features above would imply the claimed limitations to detect wafer mark alignment on the semiconductor body." However, Nishi does not teach or suggest the limitations of claim 17. Since the reference does not teach the claimed limitations, and the Final Rejection has provided no rationale as to any modification to the prior art could be made, Appellant respectfully submits that claim 17 is allowable.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of claims 4-17 under 35 U.S.C. § 103 is improper and respectfully requests that the Board of Patent Appeals and Interference so find and reverse the Examiner's rejections.

To the extent necessary, Appellant petitions for an Extension of Time under 37 C.F.R. 1.136. Please charge any fees, or credit any overpayments, in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 50-1065.

Respectfully submitted,



Ira S. Matsil
Attorney for Appellant
Reg. No. 35,272

Slater & Matsil, L.L.P.
17950 Preston Road, Suite 1000
Dallas, TX 75252
ph: (972) 732-1001
fax: (972) 732-9218

APPENDIX

ALL PENDING CLAIMS

1-3. Cancelled

4. (Previously Presented) Apparatus for detecting an alignment mark on a semiconductor body, such alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship, such apparatus comprising:

an optical system for scanning an alignment illumination comprising a pair of orthogonal lines of impinging light over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of laterally displaced beams of reflected light; and

a pair of laterally spaced detectors, each one of the detectors being positioned to detect a corresponding one of the laterally displaced beams of reflected light.

5. (Previously Presented) The apparatus of claim 4, wherein a first impinging light line is projected onto the wafer surface at an angle of -45° with respect to a Y axis, the Y axis orthogonal to the lower and top outer peripheral portion of the semiconductor body.

6. (Previously Presented) The apparatus of claim 5, wherein a second impinging light line is projected onto the wafer surface at an angle of +45° angle with respect to the Y axis.

7. (Previously Presented) The apparatus of claim 6, wherein the alignment light lines are separated laterally along the X axis by a distance W.

8. (Previously Presented) The apparatus of claim 7, wherein the alignment marks are scanned first by the light line with +45° orientation and subsequently by the line with -45° orientation.

9. (Previously Presented) The apparatus of claim 4, wherein the parallel lines comprise grooves having sidewalls terminating at the surface of the semiconductor body.

10. (Previously Presented) The apparatus of claim 9, wherein the grooves have bottomed portions recessed into the surface portion of the wafer body.

11. (Previously Presented) The apparatus of claim 4, wherein the apparatus comprises a detector arrangement.

12. (Previously Presented) The apparatus of claim 11, wherein the arrangement comprises a pair of detector configurations.

13. (Previously Presented) The apparatus of claim 12, wherein the configuration comprises a pair of detectors.

14. (Previously Presented) The apparatus of claim 13, wherein a first detector configuration comprises a first detector for detecting left +45° and a second detector for detecting right +45° lines.

15. (Previously Presented) The apparatus of claim 14, wherein a second detector configuration comprises a first detector for detecting left -45° and a second detector for detecting right -45° lines.

16. (Previously Presented) The apparatus of claim 13, wherein the pair of detectors record one or more waveforms.

17. (Previously Presented) The apparatus of claim 16, wherein the recorded waveforms are recorded without background noise from the other line orientation.